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<u>L20</u>	l3 and boolean	16	<u>L20</u>
<u>L19</u>	L17 and l6	24	<u>L19</u>
<u>L18</u>	L17 and l5	183	<u>L18</u>
<u>L17</u>	l2 and boolean	361	<u>L17</u>
<u>L16</u>	l4 and boolean	15	<u>L16</u>
<u>L15</u>	L13 and l6	77	<u>L15</u>
<u>L14</u>	L13 and l5	579	<u>L14</u>
<u>L13</u>	L12 and (decod\$3 or predecod\$3)	1507	<u>L13</u>
<u>L12</u>	l2 and load\$5	1695	<u>L12</u>
<u>L11</u>	l2 and l5	638	<u>L11</u>

<u>L10</u>	L8 and l6	25	<u>L10</u>
<u>L9</u>	L8 and l5	80	<u>L9</u>
<u>L8</u>	load\$5 and l4	108	<u>L8</u>
<u>L7</u>	predecod\$ and l4	23	<u>L7</u>
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<u>L6</u>	(712/14,22,24,25,225)![CCLS]	1200	<u>L6</u>
<u>L5</u>	(712/2-300)[CCLS]	11287	<u>L5</u>
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<u>L4</u>	L3 and (simd or single near1 instruction\$1)	109	<u>L4</u>
<u>L3</u>	L2 and (vliw\$1 or very near1 large near1 instruction\$1)	124	<u>L3</u>
<u>L2</u>	L1 and register\$1 near2 (group\$4 or set\$1 or block\$1 or file\$1)	1914	<u>L2</u>
<u>L1</u>	(arithmetic\$3 or zero or overflow or carry or barrow or psw) near5 (flag\$4 or bit\$1) near8 condition\$3	3933	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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**1. A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, decoder**

Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; F. M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunitatsu, A.; Goto, H.; Hashi Murakami, H.; Ohtaguro, Y.; Aono, A.;

Solid-State Circuits, IEEE Journal of
Volume 34, Issue 11, Nov. 1999 Page(s):1608 - 1618

Digital Object Identifier 10.1109/4.799870

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**2. HIPAR-DSP 16, a scalable highly parallel DSP core for system on a chip: video and image processing applications**

Kloos, H.; Wittenburg, J.; Hinrichs, W.; Lieske, H.; Friebe, L.; Klar, C.; Pirsch, P.;
Acoustics, Speech, and Signal Processing, 2002. Proceedings. (ICASSP '02). IEEE International C
Volume 3, 13-17 May 2002 Page(s):III-3112 - III-3115 vol.3

Digital Object Identifier 10.1109/ICASSP.2002.1005346

[AbstractPlus](#) | Full Text: [PDF](#)(562 KB) IEEE CNF

**3. Hipar-DSP-a scalable family of high performance DSP-cores**

Wittenburg, J.P.; Hinrichs, W.; Lieske, H.; Kloos, H.; Friebe, L.; Pirsch, P.;
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International
13-16 Sept. 2000 Page(s):92 - 96

Digital Object Identifier 10.1109/ASIC.2000.880682

[AbstractPlus](#) | Full Text: [PDF](#)(540 KB) IEEE CNF

**4. A 2 way VLIW processor architecture for embedded multimedia applications**

Jiyang Kang; Jae-Woo Ahn; Jiyoung Cho; Ki-Il Kum; Wonyong Sung;
Signal Processing Systems, 1999. SIPS 99. 1999 IEEE Workshop on
20-22 Oct. 1999 Page(s):211 - 220

Digital Object Identifier 10.1109/SIPS.1999.822326

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